forming a lightly-doped source/drain region with only a first dopant, the lightly-doped source/drain region located between first and second isolation structures; and creating a gate over the lightly-doped source/drain region.

- The method as recited in Claim 1 wherein forming includes forming (Original) a lightly-doped source/drain region with a first N-type dopant.
- (Original) The method as recited in Claim 2 wherein the first N-type dopant has an implant dose ranging from about 1E12 atoms/cm2 to about 1E13 atoms/cm2.
- The method as recited in Claim 3 wherein the first N-type dopant has an implant dose of about 5E12 atoms/cm².
- The method as recited in Claim 1 further including diffusing a second dopant at least partially across the lightly-doped source/drain region and under the gate to form a first portion of a channel.
- The method as recited in Claim 5 wherein diffusing the (Previously Presented) second dopant includes diffusing a P-type dopant having an implant dose ranging from about 1E13 atoms/cm2 to about 1E14 atoms/cm2.

- 7. (Previously Presented) The method as recited in Claim 5 wherein diffusing the second dopant includes diffusing a P-type dopant having an implant dose about 100 times higher than an implant dose of the first dopant.
- 8. (Original) The method as recited in Claim 5 further including placing a heavy concentration of the first dopant in a region adjacent a source side of the gate, and in the lightly-doped source/drain region adjacent a drain side of the gate.
- 9. (Original) The method as recited in Claim 8 wherein placing includes placing the heavy concentration of the first dopant in the lightly-doped source/drain region a distance ranging from about 2000 nm to about 3000 nm from the drain side of the gate.
- 10. (Original) The method as recited in Claim 8 wherein placing includes placing an implant dose of the first depart ranging from about 1E15 atoms/cm² to about 1E16 atoms/cm².
- 11. (Previously Presented) A method of manufacturing an integrated circuit, comprising:

fabricating laterally diffused metal oxide semiconductor (LDMOS) transistors, including:

forming a lightly-doped source/drain region with only a first dopant, the lightly-doped
source/drain region located between first and second isolation structures; and
creating a gate over the lightly-doped source/drain region;
depositing interlevel dielectric layers over the LDMOS transistors; and

creating interconnect structures in the interlevel dielectric layers and interconnecting the LDMOS transistors to form an operative-integrated circuit.

- 12. (Original) The method as recited in Claim 11 wherein forming includes forming a lightly-doped source/drain region with a first N-type dopant.
- 13. (Original) The method as recited in Claim 12 wherein the first N-type dopant has an implant dose ranging from about 1E12 atoms/cm² to about 1E13 atoms/cm².
- 14. (Original) The method as recited in Claim 13 wherein the first N-type dopant has an implant dose of about 5E12 atoms/cm².
- 15. (Original) The method as recited in Claim 11 further including diffusing a second depart at least partially across the lightly-doped source/drain region and under the gate to form a first portion of a channel.
- 16. (Previously Presented) The method as recited in Claim 15 wherein diffusing the second dopant includes diffusing a P-type dopant having an implant dose ranging from about 1E13 atoms/cm² to about 1E14 atoms/cm².